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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/747,621	12/30/2003	Byeong Ryeol Lee	040008-0307457	2865

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EXAMINER	
JEFFERSON, QUOVAUNDA	
ART UNIT	**PAPER NUMBER**
2823	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/15/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/747,621	LEE, BYEONG RYEOL	
	Examiner	Art Unit	
	Quovaunda Jefferson	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smayling et al, US Patent 5,348,895, in view of Yoo et al, US Patent 5,858,830.

Regarding claim 1, Smayling teaches a method of forming device isolation structures in an embedded semiconductor device comprising the steps of providing a semiconductor substrate **150** having a first area **147** for a power device and a second area **139, 140** for a logic device, forming a first device isolation region **210** in the first area, forming a first type well **154** with deep junction by diffusion of ions in the first area forming a device isolation region **210** in a second area of the semiconductor substrate, forming a first type well **175** with shallow junction in peripheral regions of the device isolation structure (**210 on left side of area 139)** and a region between the device isolation structure (**210 on right side of area 147)** and the device isolation structure (**210 on left side of area 139)**, forming a second type well **161, 190** with shallow

junction in peripheral regions of the device isolation structure (**210 in area 147)** and a region of the device isolation structure (**210 in area 140)**, and defining first and second type active regions (**areas between isolation regions 210**) on the semiconductor substrate (see figure 2i, table 1, and column 11, lines 10-35).

Smayling fails to teach forming a device isolation region through partial oxidation and forming a second device isolation with a trench in the second area of the semiconductor substrate.

Yoo teaches forming a device isolation region through partial oxidation (abstract and column 1, lines 40-43) by teaching that traditional memory cells have been fabricated using thermally grown field oxide regions by a thermal oxidation, and forming a second device isolation **11** with a trench in the second area **2** of the semiconductor substrate (column 1, lines 40-47 and figure 7) by teaching the formation of a trench isolation formation within a MOSFET logic devices and field oxide regions within a memory devices because while field oxides offers acceptable junction leakage needed for memory type devices, trench isolations regions offers greater protection against latch0up phenomena than the LOCOS and field oxide counterparts.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yoo with that of Smayling because traditional memory cells have been fabricated using thermally grown field oxide regions by a

thermal oxidation and while field oxides offers acceptable junction leakage needed for memory type devices, trench isolations regions offers greater protection against latch-up phenomena than the LOCOS and field oxide counterparts.

Regarding claim 3, Smayling teaches the first type well is an n-type well and the second type well is a p-type well (figure 2k).

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smayling and Yoo as applied to claim 1 above, and further in view of Bohr et al, US Patent 5,091,332.

Regarding claim 2, Smayling and Yoo fail to teach diffusion of ions is simultaneously conducted when the partial oxidation is performed.

Bohr teaches diffusion of ions is simultaneously conducted when the partial oxidation is performed (column 2, lines 7-10 and column 3, line 63 to column 4, lines 18) by teaching the formation of a field oxide region during the oxidation step, which simultaneously causes the implanted ions to diffuse during the formation of the field oxide. Later, another high temperature step is perform to further diffuse the ions into the substrate. The advantage of these steps is that the second high temperature step causes further diffusion of the ions to form a well without further growing the field oxide step.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Bohr with that of Smayling and Yoo because the advantage of using a wet oxidation process/dry temperature process formation is that that the second high temperature step causes further diffusion of the ions to form a well without further growing the field oxide step.

Response to Arguments

Applicant's arguments with respect to claims 1-3 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent 6,288,430, issued to Oda, discloses semiconductor device having silicide layer with silicon-rich region and method for making the same.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quovaunda Jefferson whose telephone number is 571-272-5051. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Fernando Toledo
Primary Examiner
Art Unit 2823

QVJ